CLAIMS

Amend the claims as follows.

1. (Currently Amended) A voltage generator, comprising:

a first reference voltage generator ~~capable of generating~~ to generate first and second reference voltages;

a differential amplification drive circuit ~~capable of generating~~ to generate an output voltage responsive to the first and second reference voltages and the output voltage;

a ~~resistance/diode~~ second reference voltage generator ~~capable of generating~~ to generate third and fourth reference voltages; and

a ~~pull-up/down~~ drive circuit ~~capable of changing~~ to change the output voltage responsive to the third and fourth reference voltages, the drive circuit having a first and second node, the third reference voltage connected to the first node and the fourth reference voltage connected to the second node.

2. (Currently Amended) The voltage generator of claim 1 where the first reference voltage generator comprises a plurality of serially connected ~~resistances~~ resistance elements.

3. (Currently Amended) The voltage generator of claim 1 where the differential amplification drive circuit comprises:

a first differential amplifier ~~capable of generating~~ to generate a first drive signal by comparing the second reference voltage with the output voltage;

a second differential amplifier ~~capable of generating~~ to generate a second drive signal by comparing the first reference voltage with the output voltage;

a first drive transistor ~~capable of driving~~ to drive the output voltage responsive to the first drive signal; and

a second drive transistor ~~capable of driving~~ to drive the output voltage responsive to the second drive signal.

4. (Currently Amended) The voltage generator of claim 1 where the ~~resistance/diode~~ second reference voltage generator comprises a plurality of serially connected transistors connected ~~, in turn,~~ between a voltage source and ground.

5. (Original) The voltage generator of claim 4 where the serially connected transistors are MOS transistors.

6. (Currently Amended) The voltage generator of claim 5 where the ~~resistance/diode~~ second reference voltage generator generates the third and fourth reference voltages according to a size of the serially connected MOS transistors.

7. (Currently Amended) The voltage generator of claim 1 where the ~~pull-up/down~~ drive circuit comprises a plurality of serially connected transistors commonly connected to the output voltage.

8. (Original) The voltage generator of claim 1 where the first reference voltage has a voltage level greater than the second reference voltage.

9. (Currently Amended) A voltage generator, comprising:

a first resistance element connected between a power terminal and a first node;

a second resistance element connected between the first node and a second node;

a third resistance element coupled between the second node and a ground terminal;

a first differential amplifier having a first input connected to the second ~~second~~ node and a second input connected to an output terminal;

a second differential amplifier having a first input connected to the first node and a second input connected to the output terminal;

a first pMOS transistor having a source, drain, and gate, the source being connected to the power terminal, the drain being connected to the output terminal, and the gate being connected to an output of the first differential amplifier;

a first nMOS transistor having a source, drain, and gate, the source being connected to the ground terminal, the drain being connected to the output terminal, and the gate being connected to an output of the second differential amplifier;

a second nMOS transistor having a source, drain, and gate, the source being connected to the output terminal and the drain being connected to the power terminal;

a second pMOS transistor having a source, drain, and gate, the source being connected to the output terminal and the drain being connected to the ground terminal;

a third pMOS transistor having a source, drain, and gate, the source being connected to the power terminal, the drain being connected to a gate of the second nMOS transistor, and the gate being connected to the output terminal;

a third nMOS transistor having a source, drain, and gate, the drain and gate being commonly connected to the drain of the third pMOS transistor;

a fourth pMOS transistor having a source, drain, and gate, the source being connected to a source of the third nMOS transistor and the gate and drain are commonly connected to the gate of the second pMOS transistor; and

a fourth nMOS transistor having a source, drain, and gate, the source being connected to the ground terminal, the drain being connected to the drain of the fourth pMOS transistor, and the gate being connected to the output terminal.

10. (Currently Amended) A voltage generator, comprising:

a first resistance element connected between a power terminal and a first node;

a second resistance element coupled between the first node and a second node;

a third resistance element coupled between the second node and a ground terminal;

a first differential amplifier having a first input connected to the second node and a second input directly connected to an output terminal;

a second differential amplifier having a first input connected to the first node and a second input directly connected to the output terminal;

a first pMOS transistor having a source, drain, and gate, the source being connected to the power terminal, the drain being connected to the output terminal, and the gate being connected with an output of the first differential amplifier;

a first nMOS transistor having a source, drain, and gate, the source being connected to the output terminal, the drain being connected to the ground terminal, and the gate being connected to an output of the second differential amplifier;

a fourth resistance element connected between the power terminal and the output terminal; and

a fifth resistance element connected between the output terminal and the ground terminal.

11. (Currently Amended) ~~The generator of claim 10 where the fourth and fifth resistances are N-type MOS diodes.~~ A voltage generator, comprising:

a first resistance element connected between a power terminal and a first node;

a second resistance element coupled between the first node and a second node;

a third resistance element coupled between the second node and a ground terminal;

a first differential amplifier having a first input connected to the second node and a second input directly connected to an output terminal;

a second differential amplifier having a first input connected to the first node and a second input directly connected to the output terminal;

a first pMOS transistor having a source, drain, and gate, the source being connected to the power terminal, the drain being connected to the output terminal, and the gate being connected with an output of the first differential amplifier;

a first nMOS transistor having a source, drain, and gate, the source being connected to the output terminal, the drain being connected to the ground terminal, and the gate being connected to an output of the second differential amplifier;

a first N-type MOS diode connected between the power terminal and the output terminal; and

a second N-type MOS diode connected between the output terminal and the ground terminal.

12. (Currently Amended) ~~The generator of claim 10 where the fourth and fifth resistances are P-type MOS diodes.~~ A voltage generator, comprising:

a first resistance element connected between a power terminal and a first node;

a second resistance element coupled between the first node and a second node;

a third resistance element coupled between the second node and a ground terminal;

a first differential amplifier having a first input connected to the second node and a second input directly connected to an output terminal;

a second differential amplifier having a first input connected to the first node and a second input directly connected to the output terminal;

a first pMOS transistor having a source, drain, and gate, the source being connected to the power terminal, the drain being connected to the output terminal, and the gate being connected with an output of the first differential amplifier;

a first nMOS transistor having a source, drain, and gate, the source being connected to the output terminal, the drain being connected to the ground terminal, and the gate being connected to an output of the second differential amplifier;

a first P-type MOS diode connected between the power terminal and the output terminal; and

a second P-type MOS diode connected between the output terminal and the ground terminal.

Add the following new claims.

13. (New) The generator of claim 10 where the fourth and fifth resistance elements are N-type MOS diodes.

14. (New) The generator of claim 10 where the fourth and fifth resistance elements are P-type MOS diodes.

15. (New) The voltage generator of claim 1 where the second reference voltage generator comprises a plurality of serially connected resistance elements.